REMARKS

Claims 2, 8, and 9 have been cancelled. Claims 1, 3-7 and 10 remain pending in this application. Applicants cancel claim 8 and incorporate its features in amended claims 7 and 10. Applicants also amend claim 1 to incorporate features corresponding to those recited in claim 7. No new matter has been added.

Applicants acknowledge with appreciation the Examiner's indication that claims 4-6 contain allowable subject matter. There are no outstanding objections or rejections to these claims. As such, Applicants respectfully request that the Examiner allow these claims. Applicants further submit that the reasons for allowability provided include only the Examiner's interpretation, which should in no way limit the scope of the allowable claims.

Claims 1, 3, 7, and 10 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,715,276 to Tran et al.; claim 8 was rejected under 35 U.S.C. §103(a) as being unpatentable over Tran et al. Applicants cancel claim 8 and incorporate its features in claims 7 and 10. Applicants also amend claim 1 to incorporate features corresponding to claim 7. The Examiner's rejection is respectfully traversed.

The Examiner applied the description of a first plurality of shift registers 131 and a second plurality of shift registers 132 in Tran et al. as alleged disclosure of the claimed first and second code registers. The Examiner further contended that the need for aligning the shift registers 131 and 132 renders obvious the claimed feature of setting a second signal to a phase while correlation calculation is being performed on a first signal.

Tran et al. describe an arrangement that achieves multiplexed process by performing double-rate processing within a chip cycle. To this end, the arrangement includes the first and second plurality of shift registers 131 and 132, and switches between the two, as shown in Fig. 11. In the first half of the clock period, the first plurality of shift registers 131 are selected to correlate with the 256 input samples. Please see col. 24, lines 18-20 of Tran et al. In the second half of the clock period, the second plurality of shift registers 132 are selected to correlate with the same set of 256 input samples. Please see col. 25, lines 30-32 of Tran et al. Thus, the first and second plurality of shift registers 131 and 132 are used for correlating with the same set of input samples over the respective first and second half of a clock period. As such, shifting input samples stored in the data shift registers 134 to set new samples while correlation calculation is being performed would undermine the intended operations and the objectives of the circuit arrangement described in Tran et al., which is to correlate with the same set of input samples over respective first and second half of a clock period. In other words, Tran et al. teach away from the claimed feature of "said second shift register shifts the second received signal to set the second received signal to a predetermined phase while correlation calculation is being performed for the first received signal," as recited in claims 7 and 10.

Accordingly, Applicants respectfully submit that claims 7 and 10 are patentable over Tran et al. for at least the above-stated reasons. Claim 1 includes features that correspond to those of claims 7 and 10 discussed above, and is, therefore, together with claim 3 dependent therefrom, patentable over Tran et al. for at least the same reasons.

Claims 1, 3, 7, 8, and 10 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,999,562 to Hennedy et al. The Examiner's rejection is respectfully traversed.

Again, the cited portions of Hennedy et al. disclose in-phase and quadrature-phase shift registers for outputting I and Q terms, respectively, that are matched filter correlated with a local reference signal stored in a data reference signal register, where the system is activated only during peak correlation periods.

The Examiner acknowledged that Hennedy et al. do not disclose "said at least one code register includes a first code register storing a first de-spreading code and a second code register storing a second de-spreading code." Page, 7, lines 6-8 of the Office Action. The Examiner contended, however, that the data reference signal register described therein, together with the multiplexer connected to its parallel outputs, is functionally equivalent to two separate code signal registers. The Examiner further cited col. 27, lines 60-65 of Hennedy et al. as alleged description of "I_SIG" and "Q_SIG" codes being stored in the code register. Such portions of Hennedy et al. do not, however, describe the "I_SIG" and "Q_SIG" codes being stored in the data reference signal register, as contended by the Examiner. The cited portions merely describe the data stored in the data reference signal register being used to correlate with the data contained in the "I_SIG" and "Q_SIG" registers. Although Hennedy et al. does appear to disclose multiplexing local reference signals, these signals are stored and originate from the data reference signal register, which is a single shift register with its parallel outputs coupled to a multiplexer. As such, the contents of this single shift register is continuously changed "in a

bursty mode." Col. 28, lines 4-11 of Hennedy et al. Given this continuous "bursty mode" change, the single shift register described in Hennedy et al. cannot be switched instantaneously. And therefore, in view of the operational context of the continuous bursty change in the shift register, the single register cannot be functionally equivalent to two separate code signal registers without making assumptions on the effects of such change to each of the two separate registers. Hennedy et al. do not provide any such assumptions or any disclosure on the effectiveness or equivalence of using two separate registers instead of the single register.

Therefore, the cited portions of Hennedy et al., relied upon by the Examiner, do not disclose or suggest

> "a first code register storing a first de-spreading code and a second code register storing a second de-spreading code, wherein the pattern of the first de-spreading code and the pattern of the second de-spreading code are different, and said apparatus further comprising a selector which selects one of said first code register and said second code register to select and supply the de-spreading-code sequence to the multiplication circuit," as recited in claim 1. (Emphasis added)

Again, the claimed invention advantageously provides for instantaneous code switching for the de-spreading codes, whereas the contents of the data reference signal register disclosed in Hennedy et al. are changed continuously and does not provide for such instantaneous code switching.

Accordingly, it is respectfully submitted that claim 1, together with claim 3 dependent therefrom, is patentable over Hennedy et al. Claims 7 and 10 include features that correspond to

those from claim 1 discussed above. They are, therefore, patentable over Hennedy et al. for at least the same reasons.

Statements appearing above in respect to the disclosures in the cited references represent the present opinions of the undersigned attorney and, in the event that the Examiner disagrees with any of such opinions, it is respectfully requested that the Examiner specifically indicate those portions of the respective reference providing the basis for a contrary view.

It is respectfully submitted that the present claims are in condition for allowance. Accordingly, favorable reconsideration of this case and early issuance of a Notice of Allowance are respectfully requested.

Any fee due with this paper may be charged on Deposit Account 50-1290.

Respectfully submitted

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